IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-20, NO. 1, FEBRUARY 1985

Development of the Self-Aligned-Titanium Silicide Process for VLSI Applications

MICHAEL E. ALPERIN, THOMAS C. HOLLAWAY, ROGER A. HAKEN, MEMBER, IEEE, CLAYTON D. GOSMEYER, ROBERT V. KARNAUGH, AND WALTER D. PARMANTIE, MEMBER, IEEE

Abstract—A manufacturable self-aligned titanium silicide process which simultaneously silicides both polysilicon gates and junctions has been developed for VLSI applications. The process produces silicided gates and junctions with sheet resistances of 1.0–2.0 Ω/square. This paper describes the application of the self-aligned titanium silicide process to NMOS VLSI circuits of the 64K SRAM class with 1-μm gate lengths. Comparison of circuit yield data and test structure parameters from devices fabricated with and without the silicidation process has demonstrated that the self-aligned silicide process is compatible with both VLSI NMOS and CMOS technologies.

The self-aligned titanium silicide process has some very significant manufacturing advantages over the more conventional deposited silicide on polysilicon technologies. In particular, the problems associated with etching and depositing a polycide gate stack are eliminated with the self-aligned process since the polycide etch is replaced with a much more straightforward polysilicon only etch. As gate lengths, gate oxide thicknesses, and source-drain junction depths are scaled, linewidth control, etch selectivity to the underlying gate oxide, and cross-sectional profile control become more critical. The stringent etch requirements are more easily satisfied with the self-aligned silicide process.

I. Introduction

THE USE OF polycide stacks as the gate level on MOS VLSI circuits has recently attracted much attention. The upper silicide layer reduces the sheet resistance of the stack so that the gate level may be used as a low-resistivity interconnect level while the polysilicon in contact with the gate oxide allows transistor device performance similar to that of polysilicon gate transistors [1], [2].

The self-aligned silicide process silicides the source–drain (S–D) regions and the polysilicon gates simultaneously, allowing both to be used as interconnect levels [3]–[6]. In this process a titanium film is deposited after the gates and S–D's have been fabricated and is selectively reacted with the underlying silicon regions to convert them to titanium silicide. Nitrogen is required in the reaction ambient to prevent the lateral diffusion of silicon into the titanium over oxide regions [4]. The titanium reacts with the nitrogen to form titanium nitride, which is later stripped off leaving the oxide regions free of Ti, $TiSi_2$, and TiN.

This paper describes the development of the self-aligned titanium silicide process suitable for VLSI applications using a SRAM circuit having approximately 500 000 transistors with 1-μm gate lengths, 250-Å gate oxide, and 0.2-μm self-aligned arsenic S–D's. The complexity and small physical dimensions of this circuit make it an excellent vehicle for qualifying this self-aligned titanium silicide process and fully functional silicided circuits have been fabricated.

The self-aligned process must be carefully integrated into the overall process flow to avoid potentially adverse effects on a number of device parameters. The effects of the high tensile stress resulting from the titanium silicide formation [7] may cause gate oxide integrity (GOI) problems if the silicide is too thick and the polysilicon is too thin. Also, silicide bridging between the gate and S–D regions can occur and since the S–D regions are partially converted to silicide during the process, care must be taken not to consume the junctions or degrade their diode properties. Finally, processing subsequent to the silicide formation must be considered so that the silicide sheet resistance and metal to silicide contact resistance are not degraded.

In Section II, the self-aligned silicide process is compared to deposited silicide technologies and reasons are given for it being the more manufacturable process. Section III contains details of the silicide process. The effects of the silicide process on discrete device parameters are considered in Section IV. This section is divided into subsections which address sheet resistance, contact resistance, diode leakage, GOI, and gate-to-S–D isolation. Silicided transistor characteristics are displayed in Section V, and Section VI features conclusions and a discussion.

II. Choice of Silicide Technology

The self-aligned silicide process has some very significant manufacturing advantages over the more conventional deposited silicide on polysilcon technologies. The self-aligned silicide is selectively formed on gate and S–D regions after they are fabricated, in contrast to deposited silicides, which are deposited on the polysilicon film prior to gate patterning. Thus all problems associated with etching silicide/polysilicon (polycide) stacks are circumvented

Manuscript received July 6, 1984; revised September 17, 1984.

M. E. Alperin was with Texas Instruments, Inc., Dallas, TX. He is now with INMOS, Colorado Springs, CO.
T. C. Holloway and R. A. Haken are with the Semiconductor Process and Design Center, Texas Instruments, Inc., Dallas, TX 75265.
C. D. Gosmeyer was with Texas Instruments, Inc., Dallas, TX. He is now with Hewlett Packard, Santa Rosa, CA.
R. V. Karnaugh was with Texas Instruments, Inc., Dallas, TX. He is now with Advanced Facilities, Inc., Dallas, TX.
W. D. Parmantie was with Texas Instruments, Inc., Dallas, TX. He is now with Advanced Micro Devices, San Antonio, TX.

0018-9200/85/0200-0061$01.00 ©1985 IEEE

since the silicide is not formed until after the gate level is etched. This is a very important advantage because the etch requirements are difficult to meet for VLSI products with 1-μm gate lengths and 250-Å gate oxide thicknesses. Gate etches must produce features very close to the same size as the resist pattern and with a near vertical profile without leaving residues or removing the thin gate oxide beneath the polysilicon. These requirements help ensure that linewidth control tolerances can be met, that the self-aligned S–D implant is not masked by a gate edge with a negative slope and that the S–D regions are not etched or pitted. Many polycide etches are sensitive to silicide stoichiometry, purity, and microstructure as well as silicide–polysilicon interface cleanliness. This has made it difficult to develop silicide deposition and polycide etch processes which allow all of the etch requirements to be met. With the self-aligned titanium silicide process they are more easily satisfied since only a polysilicon film is etched.

Deposition requirements are also easily met. The relatively straightforward titanium deposition can be done with a readily obtained high-purity target. In addition, if oxygen is incorporated in the deposited film, it is expelled during silicide formation [10], [11]. Because of the high purity of silicide films formed with this process, resistivity values in the reported bulk resistivity range, 13–16 $\mu\Omega$-cm [12], can be achieved. Since titanium silicide has a lower resistivity than any of the other refractory metal silicides, sheet resistances of 1–2 Ω/square can be obtained.

The self-aligned process has been developed with future silicide requirements, as well as manufacturability, in mind. CMOS, which is likely to become the dominant MOS VLSI technology, will require both low sheet resistance junctions and polysilicon gates. For CMOS with 2 μm and below gate lengths the high-resistance p^+ S–D's should be silicided if the full performance advantages of scaled p-channel devices are to be realized. The high p^+ sheet resistivity, at $\sim$100 Ω/square, limits p-channel packing density for drivers, prevents the p^+ junctions from being used efficiently as interconnects, and results in high contact resistance [4], [8]. For VLSI scaled CMOS, the most important application of silicides may be the silicidation of junctions since long distance interconnects will be implemented with a low-resistivity metal where possible [9].

III. Baseline Silicide Process Details

After the heavily phosphorus-doped 4500-Å polysilicon gate is etched, the self-aligned reachthrough implant is done, using the gate as an implant mask. The reachthrough implant forms a lightly doped drain extension (LDD) to minimize hot-electron effects. Then the gate sidewall oxide is formed by depositing an LPCVD oxide and anisotropically plasma etching it to leave filaments on the gate sidewalls. The sidewall oxide serves as an implant mask during the formation of the self-aligned S–D's and prevents the silicide from shorting gates and S–D's together across the thin gate oxide. The exposed gate oxide is also removed during the sidewall oxide etch, leaving the gate

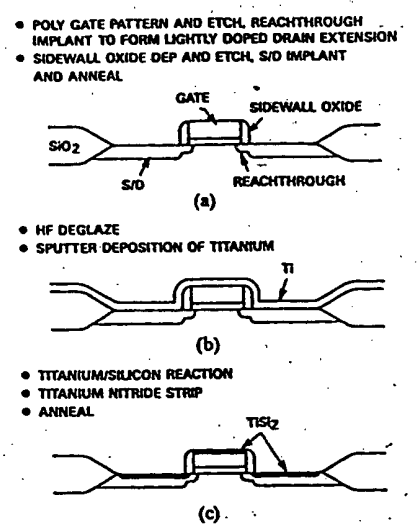


Fig. 1. Self-aligned titanium–silicide process flow.

and S–D regions free of oxide. Next, the S–D's are implanted, annealed, and then driven in. It is important t drive in the junctions so that the silicide does not penetrate them. (On devices with gate lengths greater than $\sim$ 2 μm, the LDD is not required and the S–D implant can be done prior to sidewall oxide formation.) A MOS transistor structure, just prior to silicidation, is shown in Fig. 1(a).

The self-aligned silicide process involves an HF deglaze, titanium deposition, titanium–silicon reaction, titanium nitride strip, and silicide anneal. The HF deglaze is done immediately before the titanium deposition to ensure a clean interface and promote uniform reaction. 900 Å of titanium is deposited. A MOS transistor structure, after Ti deposition, is shown in Fig. 1(b).

The titanium–silicon reaction is done in a furnace tube designed specially to minimize oxygen, which readily reacts with titanium. The reaction temperature and time are critical parameters. The temperature must be high enough and the time long enough to obtain uniform and complete reaction. The upper limit for the reaction temperature is 700°C, above which titanium reacts with oxide layers to form titanium oxides [13], which are extremely difficult to remove.

The reaction proceeds in an ambient which contains nitrogen, a key ingredient in this process. Nitrogen diffuses readily into titanium [14] and reacts with the Ti to form a TiN layer, as shown in Fig. 5. The TiN effectively prevents silicon from diffusing laterally from the gate and junction regions into the titanium over oxide regions, which can result in the formation of silicide films on top of the sidewall oxides which short the gates and junctions together [4]. Following the reaction, titanium nitride and any unreacted titanium are removed with a standard sulfuric acid/hydrogen peroxide cleanup.

The silicide anneal is done in the same furnace tube in which the reaction is done. This process beings the sheet resistance down to its final value of 1.0–2.0 Ω/square. A

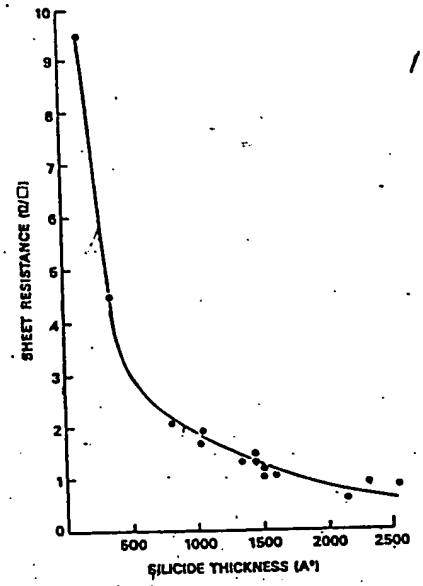


Fig. 2. Self-aligned titanium–silicide film thickness versus sheet resistance after anneal.

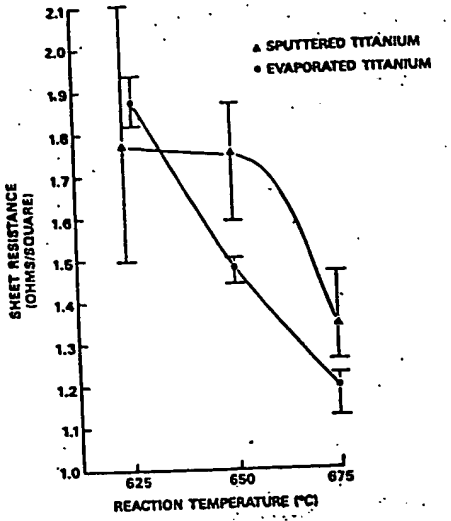


Fig. 3. Effect of Ti–Si reaction temperature on sheet resistance uniformity of films formed with sputtered and evaporated Ti. All slices had the same weight of Ti deposited on them and were reacted for 60 min.

MOS transistor structure, after silicidation, is shown in Fig. 1(c).

An LPCVD pad oxide and a PSG or BPSG layer is deposited on the silicide after formation. The metal-to-junction and metal-to-gate contacts are anisotropically etched through these layers. A rapid thermal anneal is then done to reflow the PSG or BPSG. Prior to aluminum–silicon deposition, an HF deglaze is done to ensure low and uniform contact resistance.

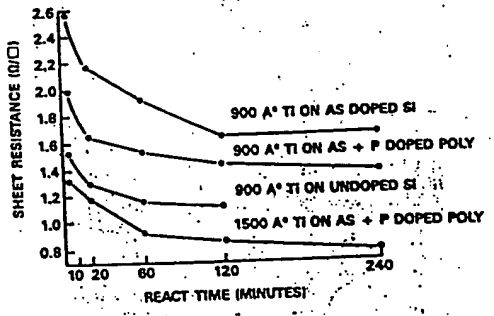


Fig. 4. Effect of substrate doping, Ti thickness, and reaction time at 675°C on silicide sheet resistance after anneal.

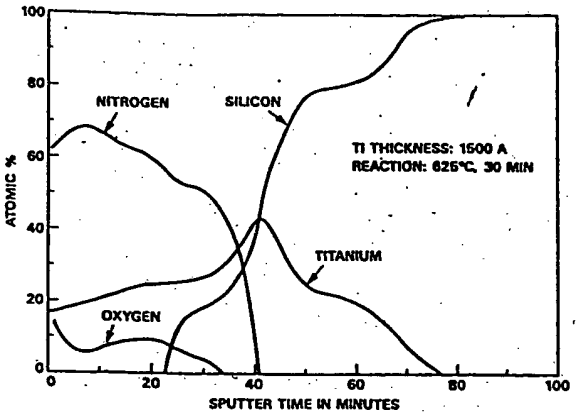
IV. Effects of Silicide on Device Parameters

A: Silicide Formation and Sheet Resistance

Sheet resistance is the most important property of a silicide film and is usually the first that is optimized when a process is developed. It is influenced by substrate type, substrate dopant species and concentration, cleanliness of the titanium–silicon interface, titanium thickness and density, titanium deposition conditions, reaction conditions, annealing conditions, and degradation of the film during subsequent processing. In practice, the silicide sheet resistance can be controlled by a suitable choice of titanium thickness and react conditions.

The sheet resistance of a self-aligned titanium silicide film is largely determined by the thickness of the film, since resistivity variations are small with this process, Fig. 2. The silicide thickness is primarily a function of the deposited titanium film thickness and density, provided that the reaction is sufficient to allow complete reaction of the titanium film. When sputtered titanium is used, the silicide sheet resistance becomes more uniform as the reaction tends toward completion, as shown by the decreasing deviation limits in Fig. 3. The reaction is complete when additional reaction time does not cause the sheet resistance after anneal to decrease further, Fig. 4. As expected, thicker silicide films require longer reaction times.

During the reaction, silicon diffuses only part of the way through the titanium film and, therefore, does not convert all of the titanium to silicide. This is due to the presence of nitrogen in the reaction ambient, which causes two competing reactions to proceed simultaneously. While silicon diffuses into the titanium from the substrate, nitrogen diffuses in from the surface and reacts with the top layer to form titanium nitride. The silicide and nitride layers grow toward each other and nitride formation ceases when the two fronts meet, Fig. 5(a) and (b). Further reaction allows the formation of stoichiometric $TiSi_{2.0}$ throughout the silicide layer, Fig. 5(c) and (d). Where titanium is present over oxide regions, TiN is formed, preventing the formation of $TiSi_2$ very far beyond the borders of the gate and S–D regions. This prevents shorting between adjacent silicided regions since the conductive TiN film is removed during the sulfuric acid/hydrogen peroxide strip which immediately follows the reaction.

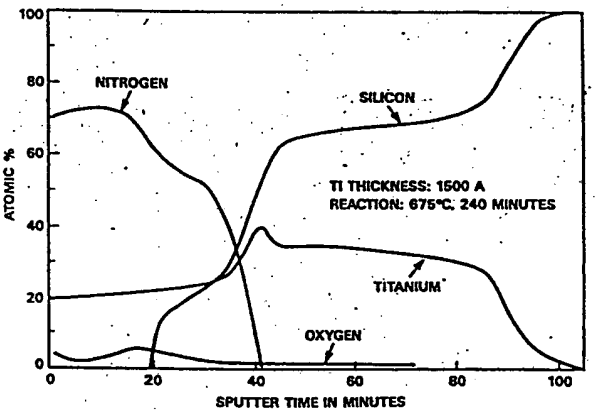


(a)

ELECTRON BAND	XPS BINDING ENERGY (eV)	MOLECULAR SPECIES INDICATED BY BINDING ENERGY
$Ti_{2p}^{3/2}$	454.8	TiN
N_{1s}	396.5	NITRIDE
O_{1s}	530.1*	METAL OXIDE

*USED AS CALIBRATION STANDARD

(b)



(c)

ELECTRON BAND	XPS BINDING ENERGY (eV)	MOLECULAR SPECIES INDICATED BY BINDING ENERGY
$Ti_{2p}^{3/2}$	454.9	TiN
N_{1s}	396.6	NITRIDE
O_{1s}	530.8*	METAL OXIDE

*USED AS CALIBRATION STANDARD

(d)

Fig. 5. Auger depth profiles of silicide films after reaction, and X-ray photoelectron spectroscopic (XPS) data taken for the surface Ti+N layers. The XPS was done with a K(sub alpha) X-ray source. (a) Before the reaction is completed a Ti+N film is present at the surface with titanium–silicide beneath it. (b) XPS results indicate that the Ti+N layer is TiN. (c) Completing the reaction allows the formation of a more stoichiometric silicide layer, but does not cause the stable titanium nitride film to grow further. (d) The surface film is again confirmed to be TiN.

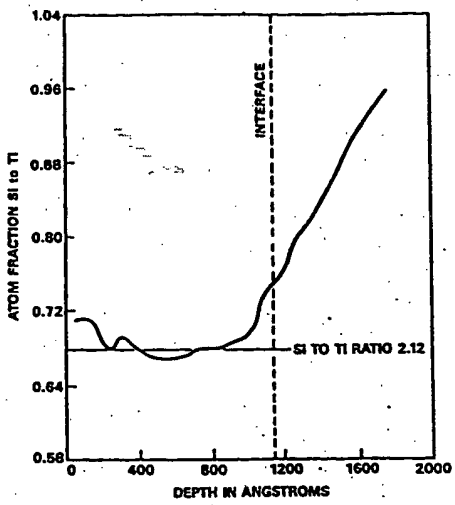


Fig. 6. RBS depth profile of a silicide film after anneal. Atom fraction equals atomic ratio/(1+atomic ratio).

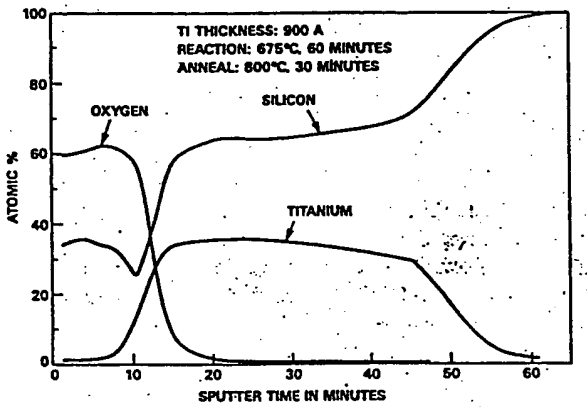


Fig. 7. Auger depth profile of a silicide film after anneal, showing the surface silicon dioxide layer which is sometimes seen.

Although the silicide film is formed during the reaction step, it does not reach its lowest resistivity until after the anneal. The resistivity is within the bulk range (13–16 Ω·cm [12]) after this step. RBS data indicate that the silicide is close to stoichiometric $TiSi_{2.0}$, Fig. 6.

Fig. 7 is an Auger depth profile of a titanium silicide film after anneal. An SiO_2 film can be seen at the surface. These films are typically 200–400 Å thick, as determined from RBS measurements. It is likely that the oxide film is the result of residual oxygen in the anneal furnace. No adverse effects have been attributed to the presence of this film.

Fig. 8 shows that the films produced with this process have a peak to valley surface roughness of approximately 300 Å. It is believed that the native oxide film at the Ti–Si interface slows down the reaction and causes it to proceed in a somewhat nonuniform fashion, resulting in a rough surface. It is also suspected that the roughness may alter the distribution of stress in the film.

The effects of substrate doping on silicide sheet resistance after anneal are illustrated in Fig. 4. The reaction is

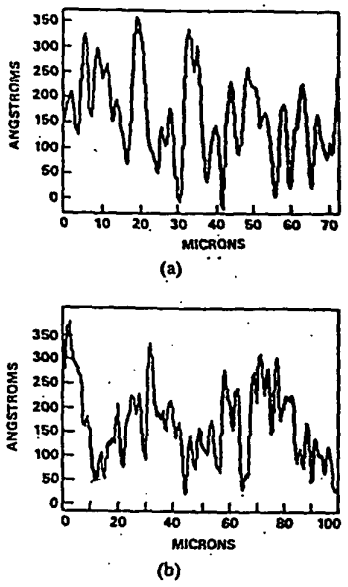


Fig. 8. Surface roughness of a silicide film after anneal, (a) on S–D and (b) on gate.

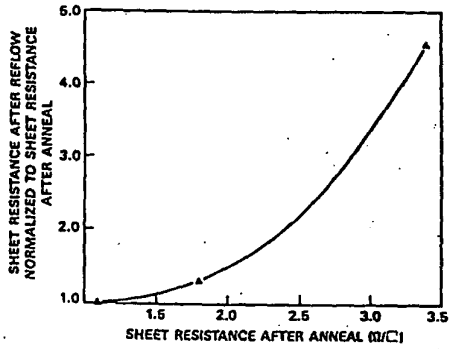


Fig. 9. Sheet resistance degradation during a 975°C PSG reflow. It can be seen that there is no degradation for films with initial sheet resistances less than 1.2 Ω/square and that the degradation increases as the initial sheet resistance does.

completed more quickly and results in lower sheet resistances on undoped single-crystal silicon than on heavily As-doped regions. This is probably because the reaction rate is lower on the doped sample. Intermediate sheet resistances are obtained on the P- and As-doped polysilicon gates.

The titanium deposition process is the last factor to be discussed that affects the reaction. The difference in final sheet resistance for films formed with sputtered and evaporated titanium is shown in Fig. 3. The differences may be due to grain size, density, or film purity. This is an area that warrants further study. Although the differences in sheet resistance and uniformity are dramatic at 625° and 650°C, they are not as great as 675°C.

The silicide sheet resitance may be degraded by processing after the anneal step. For example, the PSG reflow causes the sheet resistance to increase. The increase is dependant on the silicide sheet resistance after anneal.

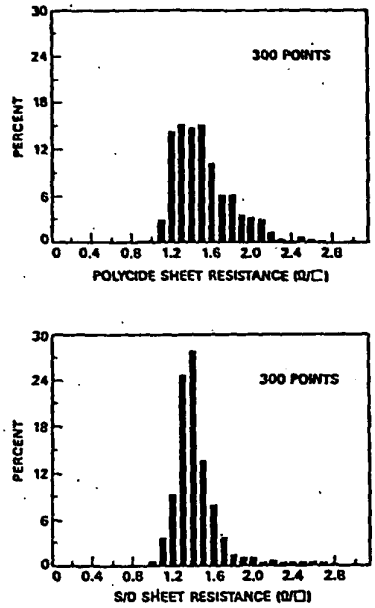


Fig. 10. Histograms of final sheet resistance. Data taken on resistors from SRAM material.

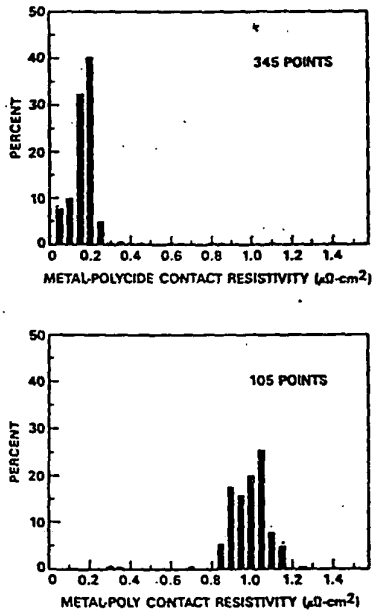


Fig. 11. Histograms of contact resistivity. Data taken on contact chains from SRAM material with 2000 2×2 μm contacts.

Fig. 9. Histograms show that sheet resistances in the range of 1.0–2.0 Ω/square are obtained at final probe on SRAM material, Fig. 10.

B. Contact Resistance

Metal-to-silicide contact resistivity for the self-aligned titanium silicide process is approximately an order of magnitude lower than that for metal to silicon contacts. Histograms of metal to polycide and metal to polysilicon contact

TABLE I
JUNCTION LEAKAGE (nA/cm²) AS A FUNCTION OF SILICIDE THICKNESS AND 975°C S–D DIFFUSION DONE PRIOR TO SILICIDE FORMATION

(Slices which received less than a 20-min diffusion prior to being silicided received a second diffusion after silicide formation so that the total diffusion time was 20 min.)

SOURCE/DRAIN DRIVE-IN TIME (minutes) \ SILICIDE THICKNESS (angstroms)	0	325	750	1100	1375	1500
5	7050	26	26	9	1100	2650
10	26	9	35	22	22	26
15	9	9	18	9	22	9
20	9	9	26	13	13	13

resistivity are compared in Fig. 11. The polysilicon used for both the polycide and the polysilicon contact structures is 0.5 μm thick and doped with phosphorus to 20 Ω/square. Two terminal resistance measurements were made on a large number of contact chains, each having 2000, 2×2 μm contacts. After subtracting series sheet resistances, the contact resistivities were determined from the resistance of a contact of known size. An HF contact deglaze is done, prior to aluminum deposition, to ensure low and uniform contact resistance.

C. Diode Leakage

Junction diode leakage is a concern since the S–D junctions are partially converted to silicide in the self-aligned process. In order to achieve good junction integrity, the S–D's must be annealed and driven in prior to silicide formation. Table I shows the effects of S–D diffusion time and silicide thickness on junction leakage currents. Measurements were made on a gated diode test structure with an S–D junction area of 2.27 E-4 cm². The surface under the gate was accumulated. When a 5-min diffusion is done, silicides thicker than 1100 Å cause gross leakage problems. Since it is known that arsenic does not significantly redistribute during titanium silicide reaction [15], the gross leakage problem may be due to differences in subsequent diffusion of arsenic from the titanium–silicide layer resulting in shallower junction depths than if the arsenic is diffused before silicide formation. The lower leakages of the silicided junctions as compared to the unsilicided junctions may be due to impurity gettering taking place during silicide formation. For diffusions greater than 5 min, low leakage is exhibited with silicide films up to 1500 Å thick.

Because the gated diode structure does not have S–D junctions that extend to the field-oxide edge, a second structure which does, has also been characterized. This standard diode has an S–D junction area of 2.25 E-5 cm² and an S–D to field perimeter of 4.8 E-2 cm.

On one batch of material, the effects of increasing the silicide thickness above 1500 Å were examined. The data is displayed in Table II. Although the "background" leakage is higher than on other lots, no increase in leakage is seen for silicides as thick as 2000 Å. This is somewhat surprising since modeling indicates that the S–D junctions are only 2000 Å deep. It seems that the silicide thickness may closely approach the junction depth before leakage problems are encountered. (Again, high leakage is seen on the unsilicided control slices.)

TABLE II
EFFECT OF SILICIDE THICKNESS ON JUNCTION LEAKAGE
(Total diffusion time of 20 min at 975°C used on all splits.)

	SPLIT 1 (control, unsilicided)	SPLIT 2 (baseline process)	SPLIT 3	SPLIT 4
NUMBER OF BARS TESTED	60	180	90	90
S/D SHEET RESISTANCE (ohms/square)	26.0	1.4	0.9	0.8
CALCULATED THICKNESS (angstroms)*	–	1150	1775	2000
JUNCTION LEAKAGE: (nA/cm²)				
GATED DIODE	163	20	25	19
STANDARD DIODE	162	95	134	115

*SILICIDE THICKNESS CALCULATED ASSUMING A RESISTIVITY OF 16 $\mu\Omega$-cm

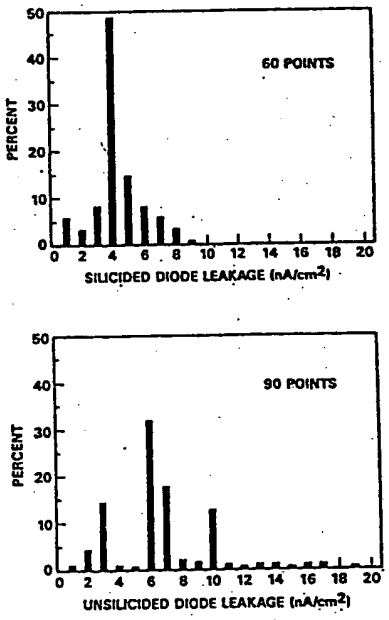


Fig. 12. Histograms of diode leakage. Data taken on standard diodes from SRAM material.

Histograms of junction leakage for silicided and unsilicided slices are shown in Fig. 12. This data are taken from SRAM material. There is no significant difference in leakage between the silicided junctions and the unsilicided junctions. The successful fabrication of VLSI circuits, which have 2.5 m of gate-to-S–D junction edge, is also a good indication that there are no diode leakage problems associated with junction silicidation.

D. Gate Oxide Integrity and Gate-to-Junction Shorting

Data from several batches of completely processed material indicates that the GOI is excellent on both silicided and unsilicided slices, Fig. 13. The test structure used contains 2.02 E-3-cm² poly(cide) fingers on gate oxide. Between the fingers are (silicided) junctions regions.

TABLE III
EFFECTS OF SILICIDE THICKNESS ON GOI AND GATE-TO-S–D ISOLATION

	SPLIT 1 (control, unsilicided)	SPLIT 2 (baseline process)	SPLIT 3	SPLIT 4
NUMBER OF BARS TESTED	60	180	90	90
POLYCIDE SHEET RESISTANCE (ohms/square)	25.5	1.2	0.9	0.8
CALCULATED SILICIDE THICKNESS (angstroms)*	–	1325	1775	2000
POLY THICKNESS (angstroms)	4500	3425	3060	2880
GATE OXIDE INTEGRITY (defects/cm²)	§	§	103	321
(% fail @ < 7 V)	0	2	19	48
% S/D TO GATE SHORTING	0	1.3	1.1	0

* SILICIDE THICKNESS CALCULATED ASSUMING A RESISTIVITY OF 16-Ω-cm

§ A MEANINGFUL VALUE IN DEFECTS/cm² CANNOT BE CALCULATED DUE TO THE RESOLUTION OF THE TEST STRUCTURE. THERE IS PROBABLY NO SIGNIFICANT DIFFERENCE IN GOI BETWEEN SPLIT 1 AND SPLIT 2.

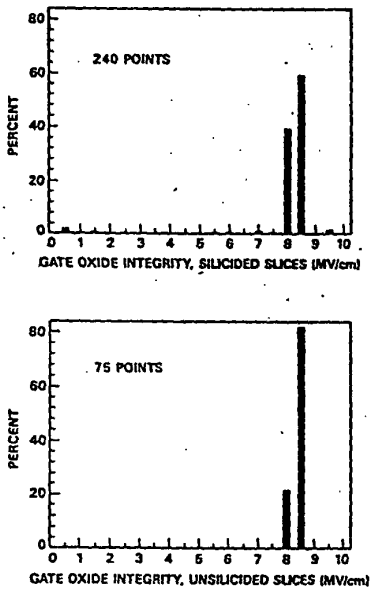


Fig. 13. Histograms of GOI. Data taken on fingered capacitors from SRAM material.

Titanium–silicide films have a high stress, which can result in gate oxide integrity failures [2]. In Table III, it can be seen that the unsilicided control slices and the slices which received the baseline silicide process have similar GOI. As the silicide thickness is increased and the polysilicon thickness decreases, the GOI is compromised. Even for the thickest silicides, at 0.8 Ω/square, gate-to-junction shorting across the sidewall oxide, however, is not observed.

V. TRANSISTOR CHARACTERISTICS

Histograms of natural device threshold voltages and subthreshold slopes are shown in Figs. 14 and 15 for silicided and unsilicided slices. Table IV compares average values of S–D series resistance, threshold voltage, subthreshold slope, and drive currents for natural transistors. Enhancement device I–V curves are displayed in Fig. 16. As can be seen, there is very little difference between the silicided and unsilicided transistors. On the test structure characterized, the drain current does not flow through an appreciable length of silicided S–D and most of the series resistance is due to the lightly doped drain extensions. Since the silicide primarily affects transistor performance

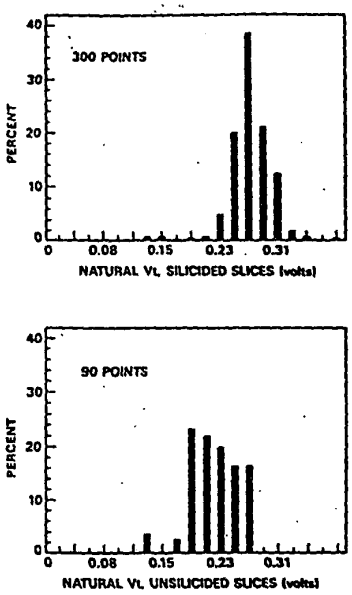


Fig. 14. Histograms of threshold voltages from SRAM material. Data taken on natural transistors with width/length ratios of 11/1 μm.

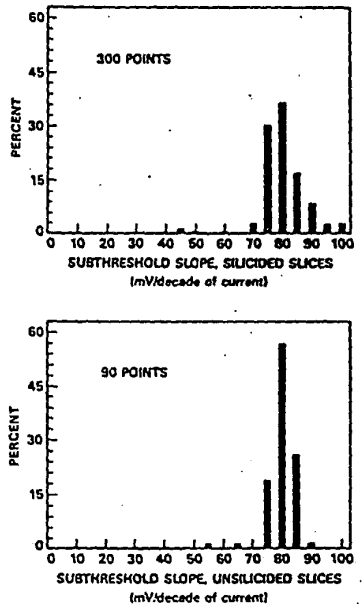
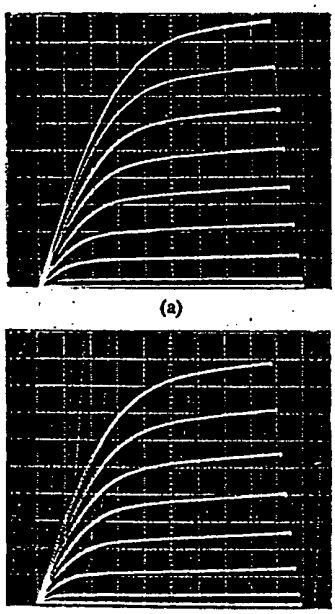


Fig. 15. Histograms of subthreshold slopes from SRAM material. Data taken on natural transistors with width/length ratios of 11/1 μm.

TABLE IV
EFFECTS OF SILICIDE ON CHARACTERISTICS OF NATURAL TRANSISTORS WITH WIDTH/LENGTH RATIOS OF 11/1 μm

	SILICIDED	UNSILICIDED
SOURCE TO DRAIN SERIES RESISTANCE (Ω)	90	103
NATURAL V_t (volts)	0.24	0.20
SUBTHRESHOLD SLOPE (mV/decade of I)	78	78
DRIVE CURRENT (mA) $V_{GS}=V_{DS}=3$ VOLTS $V_{BB}=0$ VOLTS	1.2	1.3



(a) (b)

Fig. 16. 11/1 μm enhancement transistor I–V curves, horizontal, V_D = 0.5 V/div; vertical, I_D = 250 μA/div; V_G = 0.5 V/step (V_T = 0.6 V); (a) silicided and (b) unsilicided.

by reducing the S–D series resistance, the advantages of siliciding are not realized on this particular structure. Any adverse effects of siliciding, however, would be apparent. Clearly, the silicide does not degrade transistor operation.

VI. Conclusions and Discussion

A self-aligned titanium silicide process, which simultaneously silicides both polysilicon gate and S–D junction regions, has been demonstrated on NMOS VLSI parts of the 64K SRAM class of complexity. Sheet resistances of 1.0–2.0 Ω/square have been achieved. Comparison of yield data from devices fabricated with and without the silicidation process has demonstrated that the self-aligned silicide process does not degrade device yield. This process is also of great interest in CMOS technology, to reduce the high resistance of p^+ junctions, which will introduce scaling limitations if not silicided.

The self-aligned titanium–silicide process was chosen because it has some very significant advantages over the more conventional deposited silicide on polysilcon technologies. In particular, all the problems associated with depositing a silicide film and etching a polycide gate stack are circumvented since the silicide deposition is replaced with a titanium deposition and since the polycide etch is replaced with a much more straightforward polysilicon only etch. This process, also, produces films with lower resistivities than achievable with other refractory metal silicides and allows the S–D junctions to be silicided.

Although it may be easier to produce structures with self-aligned silicides than structures with deposited silicides, it is more difficult to integrate the process into an existing device flow. It should be clear, from the results presented in this paper, that the effect of the silicide process on diode leakage, GOI, gate-to-S–D isolation, and contact resistance should be considered when the process is implemented. There are two basic requirements that must be fulfilled in order to use the current process. First, gate sidewall oxides are necessary to prevent the formation of silicide shorts between the gates and the S–D's. Second, S–D junctions should be annealed and driven in prior to silicide formation to obtain low junction leakage.

Tables II and III summarize some of the key results regarding the effect of silicide thickness on device parameters. Even for 2000-Å-thick silicides, no adverse effects are seen on the junction leakage or S–D-to-gate isolation. For silicides thicker than those obtained with the baseline process, however, GOI is compromised. Thus in the current process, GOI is the critical parameter which sets an upper limit on the silicide thickness. It is likely that the GOI degradation is due to stress in the silicide film. If thicker silicides were desired so that lower sheet resistances could be obtained, it would be a relatively simple matter to reduce the effect of silicide stress on the gate oxide by increasing the polysilicon layer thickness.

Further refinements to the self-aligned titanium silicide technology—such as ion-beam mixing [16], [17] and rapid thermal annealing [17]–[19]—may improve the silicide uniformity, allowing the sheet resistance to be extended to below 1 Ω/square. This $TiSi_2$ technology, when merged with double-level metal, may delay the need for refractory metal gate technology, at 0.5 Ω/square, to beyond the next generation of IC's. The combination of double-level metal with 1 Ω/square (or less) gate and S–D regions produces a very powerful technology that could impact high-performance CMOS products more rapidly than refractory metal gates. The self-aligned titanium silicide process also has the advantage that it is more compatible with today's MOS process technology.

Acknowledgment

Special thanks to L. Schultz for his help in processing and characterizing material. H. Tigelaar refined the Ti deposition process to produce cleaner and more uniform

films. D. Reynolds developed the software to display data in histogram form. K. Russell, with the help of A. Bowling, did the Auger and XPS analysis. The RBS was performed by J. Keenan. Also, thanks to the Texas Instruments Semiconductor Process Lab staff for processing and characterizing the self-aligned titanium–silicide material. Last, but certainly not least, the authors would like to acknowledge C. K. Lau, who did all the early development work on the self-aligned titanium–silicide process and who was eager to share his knowledge with others.

REFERENCES

[1] A. K. Sinha, "Refractory metal silicides for VLSI applications," *J. Vac. Sci. Technol.*, vol. 19, pp. 778–785, Sept.–Oct. 1981.
[2] C. Korburger *et al.*, "Electrical properties of composite evaporated silicide/polysilicon electrodes," *J. Electrochem. Soc.*, vol. 129, pp. 1307–1312, June 1982.
[3] C. K. Lau, Y. C. See, D. B. Scott, J. M. Bridges, S. M. Perna, and R. D. Davies, "Titanium disilicide self-aligned source/drain + gate technology," in *IEDM Tech. Dig.*, pp. 714–717, Dec. 1982.
[4] C. K. Lau, "Characterization of the self-aligned TiSi2 process," in *ECS Dig. Extended Abstracts*, vol. 83-1, pp. 569–570, May 1983.
[5] A. Tasch, H. S. Fu, and P. Chatterjee, "High performance submicron MOSFET device structure," U.S. Patent 4 384 301, May 17, 1983.
[6] T. Shibata *et al.*, "An optimally designed process for submicron MOSFETs," in *IEDM Tech. Dig.*, pp. 647–650, Dec. 1980.
[7] S. P. Murarka and D. B. Fraser, "Silicide formation in thin cosputtered (titanium + silicon) films on polycrystalline silicon and SiO_2," *J. Appl. Phys.*, vol. 51, p. 1593, 1980.
[8] D. B. Scott, W. R. Hunter, and H. Sichijo, "A transmission line model for silicided diffusions: Impact on the performance of VLSI circuits," *IEEE Trans. Electron Devices*, vol. ED-29, pp. 651–661, Apr. 1982.
[9] A. Mohsen, "Interconnects in VLSI," presented at the Workshop on Refractory Metal Silicides—II, San Juan Batista, CA, May 1984.
[10] A. Guldan *et al.*, "Formation and properties of $TiSi_2$ films," *Thin Solid Films*, vol. 100, pp. 1–7, 1983.
[11] P. Merchant and J. Amano, "Oxygen redistribution during sintering of Ti/Si structures," paper presented at the Workshop on Refractory Metal Silicides—II, San Juan Batista, CA, May 1984.
[12] S. P. Muraka, "Refractory silicides for integrated circuits," *J. Vac. Sci. Technol.*, vol. 17, pp. 775–792, Jul.–Aug. 1980.
[13] H. Krautle *et al.*, in *Proc. Int. Conf. Appl. Ion Beam to Metals*, (Albuquerque, NM), New York: Plenum, 1974, p. 193.
[14] A. McQuillan and M. McQuillan, *Titanium*. London: Butterworths, 1956, p. 415.
[15] M. Wittmer, C.-Y. Ting, and K. N. Tu, "Atomic motion of dopant during interfacial silicide formation," *Thin Solid Film*, vol. 104, pp. 191–195, 1983.
[16] H. Okabayashi *et al.*, "Low resistance MOS technology using self-aligned refractory silicidation," in *IEDM Tech. Dig.*, pp. 556–559, May 1982.
[17] D. Pramanik *et al.*, "Influence of the interfacial oxide on titanium silicide formation by rapid thermal annealing," paper presented at the Workshop on Refractory Metal Silicides—II, San Juan Batista, CA, May 1984.
[18] R. A. Powell, R. Chow, C. Thridandam, R. T. Fulks, I. A. Blech, and J.-D. T. Pan, "Formation of titanium silicide films by rapid thermal processing," *IEEE Electron Device Lett.*, vol. EDL-4, pp. 380–382, Oct. 1983.
[19] S. Shatas *et al.*, "HEATPULSE rapid thermal processing for annealing refractory metal silicides," paper presented at the Workshop on Refractory Metal Silicides—II, San Juan Batista, CA, May 1984.

Docket # P2001,0119

Applic. #_____

Applicant: BERNHARD SELL ET AL.

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100 Fax: (954) 925-1101

A DEEP-TRENCHED CAPACITOR TECHNOLOGY FOR 4 MEGA BIT DYNAMIC RAM

K.YAMADA, K.YAMABE, Y.TSUNASHIMA, K.IMAI, T.KASHIO and H.TANGO

VLSI Research Center, TOSHIBA Corporation
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 210, Japan
Tel 044(511)2111

Abstract

A deep-trenched capacitor technology is one of key processes for realizing 4Mb DRAM(1). Major subjects in this technology are to form a precisely controlled shallow diffusion layer at vertical side walls and to grow high reliable thin gate oxide on the trenched Si surface. In this paper, arsenic doping from As doped SiO_2 (AsSG) film into the vertical side walls and the rounding oxidation technique in O_2 ambient including a few percent H_2O, have been introduced. These techniques enable us to utilize the high-reliability trenched capacitors featuring large charge storage capability as well as low leakage current for 4Mb DRAM's.

Introduction

The memory storage capacitance for DRAM's has been maintained to be more than 35fF in order to keep soft error immunity and large S/N margin since 64Kb DRAM. According to the conventional scaling approach, the oxide thickness and capacitor area needed for 4 Mb DRAM can be estimated as about 5nm and $5um^2$, respectively. It would be quite difficult to thermally grow high reliable 5nm oxide in production environments. Instead of conventional plane capacitors, the use of trenched capacitors has attracted considerable attention (2,3). With the conventional ion implantation technique, it is extremely difficult to precisely control the doping concentration at the surface of the vertical trench side walls. And, it is well known that thermally grown oxide becomes thinner both at top convex corners and at bottom concave corners of trenches in Si, yielding high oxide leakage currents at these corners. Accordingly, major subjects in trench technology are to form precisely controlled shallow n^+ diffusion layer at vertical side walls and to obtain thin gate oxide on the trenched Si surface with low leakage current and high reliability. In this paper, in order to solve these subjects, solid phase diffusion from AsSG films and a technique to round the Si corner of the trench structure are used. The behavior of doping impurities atoms during the sequent oxidation processes is also discussed.

Device Fabrication

The trench capacitor structures were fabricated after LOCOS isolation process. The present process sequence is listed in Table 1. Deep trenches of typical sizes of 1um width and 3um depth were etched using RIE technique, where CVD SiO_2 films were used as the etching mask. The trench surfaces were then slightly etched in order to eliminate damage near the Si surfaces(4). AsSG films, in which typical As concentration is $8x10^{20}$ atoms/cm^3, were deposited on the trench vertical and bottom Si surface. Then, the shallow n^+ layer was formed by solid phase diffusion from AsSG at 1000C for 60min in N_2 ambient. The typical surface As concentration in Si is $7x10^{19}$ atoms/cm^3 after diffusion. The junction depth of 0.15um was obtained. After removing of AsSG films, the SiO_2 films of about 50nm thick were firstly grown and then stripped in diluted HF. This oxidation is performed in order

- TRENCH RIE
- DEPOSITION OF LPCVD AsSG
- As DRIVE IN
- AsSG REMOVAL
- ROUNDING OXIDATION
- GATE OXIDATION
- CONVENTIONAL PROCESS FOR MOS CAPACITORS

Table.1

Sequence of our trench capacitor process.

CH2252-5/85/0000-0702 $1.00 © 1985 IEEE

to round both the top convex and the bottom concave corners at the trenched Si edges. Thus it is called the rounding oxidation. Secondly, the gate oxide was thermally grown in H_2O diluted with argon at 900C. Poly Si films were filled into the trenches, which serves as capacitor electrodes.

Doping Technology

Arsenic is chosen as n type dopant in order to obtain the shallow n^+ diffusion layers at the trenched surface. The diffusion depth of phosphorus is approximately four times more than that of arsenic. This makes it difficult to use phosphorus as the dopant for the trench capacitor in 4Mb DRAM. Because the leakage currents between neighbouring trenches increases as the trench-trench distance is reduced below 2um. AsSG films are deposited by the simultaneous thermal decomposition of TEOS (tetra-ethoxy-silane)(5) and TEOA (tri-ethoxy-arsine) at a typical temperature of 700C in a standard LPCVD reactor. In the reactor, the TEOA decomposes to gas phase of As_2O_3 and other products. The vapour pressure of As_2O_3 depends upon the temperature and TEOA gas flow rate. This As_2O_3 gas dissolves into SiO_2 films which is continuously decomposed and deposited from TEOS onto the Si surface. Here, the As concentration in SiO_2 is in equilibrium with the gas phase of As_2O_3. Therefore, As concentration in the deposited AsSG films is independent of the AsSG deposition rate.

The surface concentration of As in Si was found to decrease during oxidation. The out-diffusion rate of As is much higher than that of calculated results considering the oxidation enhanced diffusion in silicon (6). This phenomenon, which has not been reported so far, is caused by the enhanced diffusion of As in the thin oxide and the evaporation of As from the surface of the oxide. An example of arsenic out-diffusion during oxidation is shown in Fig.1. Figure 2 shows the dependence of ($D_{As}(SiO_2)$ x m) on oxide thickness at 1000C, where $D_{As}(SiO_2)$ and m are the diffusion coefficient of As in SiO_2 and the segregation coefficient of As at SiO_2/Si interface, respectively. These experiments were carried out as follows. The (100) oriented Si wafers, having flat As profile of 1.3×10^{20} atoms/cm^3, were used as starting substrates. First, these wafers were oxidized in dry O_2 to form SiO_2 with thickness of 6 to 15nm, and then annealed in argon ambient at 1000C. The arsenic distributions were determined by SIMS measurements. The values of ($D_{As}(SiO_2)$ x m) were calculated by best fitting technique before and after the argon annealing. In Fig.3 are shown the arsenic redistributions after arsenic diffusion from AsSG (a), after rounding oxidation (b) and after gate oxidation (c). These results

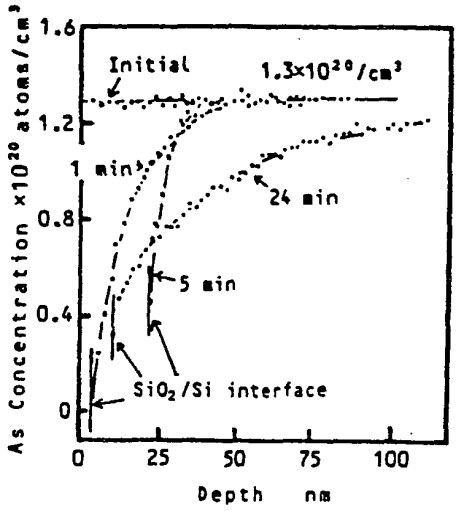


Fig.1
An example of out-diffusion of As with flat profile. Annealing ambient and temperature are O_2 and 1000°C respectively.

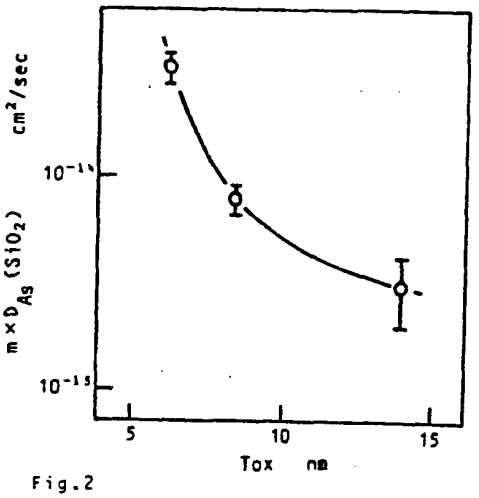


Fig.2
Relation between D_{As} in SiO_2 and oxide thichness at 1000C.
m; segregation coefficient of As at SiO_2/Si interface.

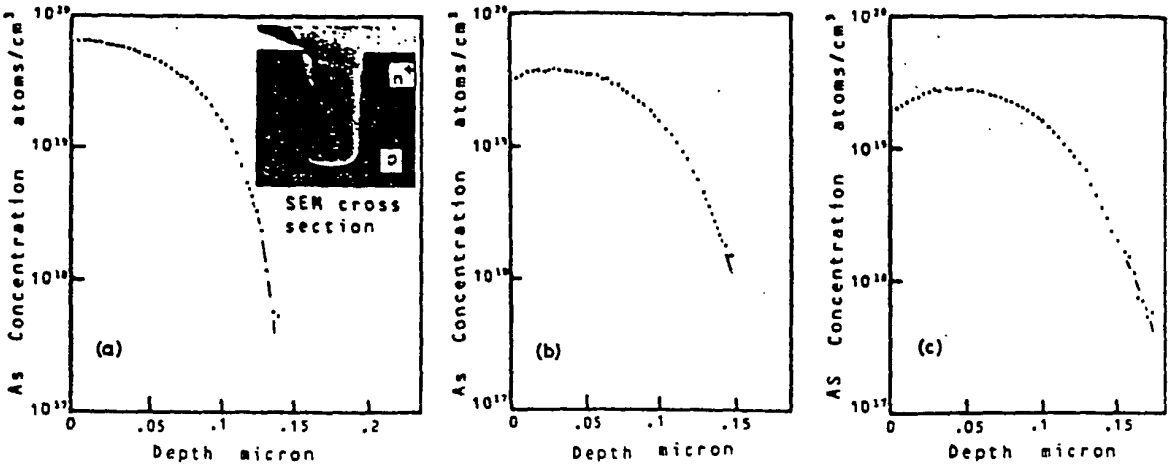


Fig. 3 As redistribution after As diffusion from AsSG(a), after rounding oxidation(b) and after gate oxidation(c). SEM cross section of diffusion layer at trenched surface. Sample of SEM was made by stain technique.

suggest that the understanding of this out-diffusion phenomenon is important in order to precisely control the n^+ layer thickness.

Rounding Oxidation

Oxide thinning at trench corners is understood as due to the compressive intrinsic stress occuring locally in the oxide film during growth. Oxide thinning effect is reduced at higher temperatures because of the stress relief by viscous flow of oxide. High temperature oxidation, however, has to be avoided in order to suppress the diffusion of the dopant. Here, we discuss the effects of oxidation ambient and impurity concentration in the Si surface on the suppression of oxide thinning. We evaluated the effect by measuring the oxide leakage current of MOS capacitors with a large trench perimeter of about 50mm and gate area of $0.1mm^2$ as shown in Fig. 4. The poly Si gate electrodes were biased positively (negatively) for n (p) type Si substrates. Since, the Si surface was in accumulation and the applied voltage appears across the oxide and oxide thinning at the convex (concave) corner edge can be evaluated by leakage current.

First, Fig. 5 shows the relationship between the leakage current and H_2O partial pressure in O_2 ambient during rounding oxidation at 950C. Decrease at the lower percentage region of H_2O can be attributed to the increase in viscous flow rate which depends on the H_2O content in SiO_2, while the increase at higher per-

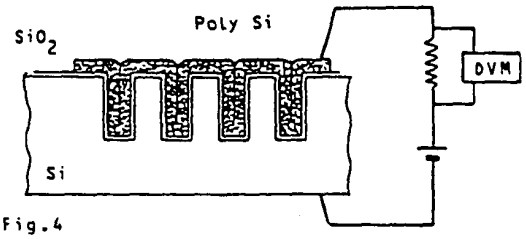


Fig.4 Automated experimental apparatus setup.

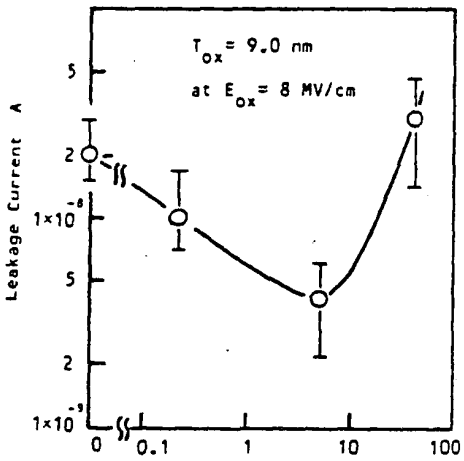


Fig.5 Relation between leakage currents and H_2O partial pressure in rounding oxidation ambient.

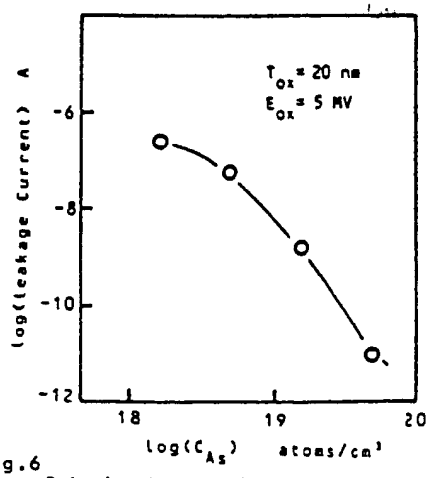


Fig.6 Relation between leakage current and As concentration of Si surface. Gate oxidation temperature is 900 °C.

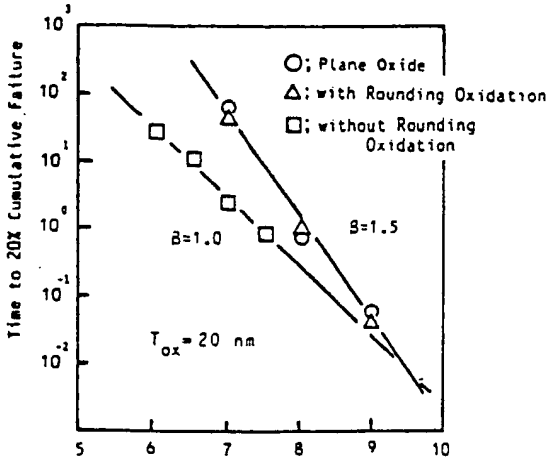


Fig.7 Time to 20% cumulative failure ,(20%), as a function of stress electric field : $F(20\%) \propto 10^{-\beta E}$

centage region is due to the high oxidation rate. Consequently, the rounding oxidation in O_2 ambient including a few percent of H_2O increases the round radius of the convex Si corner and yields the lowest oxide leakage current. On the next place, the effect of impurity concentration on the round oxidation has been investigated at 950C in dry O_2. The dependence of gate oxide leakage current on As concentration at Si surface is shown in Fig.6. The oxide leakage current decreases with increase in the As concentration. The leakage current level obtained at 5×10^{19} atoms/cm^3 is low enough to maintain the stored charge in memory capacitor. The observed rounding effect by oxidation is considered as follows: activation energy for the viscosity decreases with the increase of the concentration of hydroxyl or other impurities which are effective in breaking Si-O-Si bonds.

In Fig.7, the time to reach 20 cumulative percent failure is plotted as a function of the average stress field. The comparison is made for the 20nm thick oxides with or without the rounding oxidation. The data for the oxide grown on plane surfaces are also shown. By using the rounding oxidation technique, the electrical acceleration factor in the time dependent dielectric breakdown measurement increases from 1.0 decades/MV/cm to 1.5 decades/MV/cm which is equal to that of the plane oxide. It is concluded that the rounding oxidation is very effective to prevent the time dependent dielectric breakdown degradation in thin oxides grown on the trench structures.

Conclusion

We concluded that As doping from LPCVD AsSG into the vertical trench side walls and the corner rounding oxidation prior to gate oxidation are most promising technologies for the realization of 4 Mb DRAM with the deep-trenched capacitors. These technologies give us thin gate oxide with the low leakage current and the high reliability.

Acknowledgment

The authors wish to thank M.Kashiwagi for helpful encouragement and Miss M.Onodera for her assistance in these experiments.

References

(1) H.Ishiuchi, T.Watanabe, K.Kishi, M.Ishikawa, N.Goto, T.Tanaka, T.Mochizuki, and O.Ozawa;"Submicron CMOS Technologies for Four Mega Bit Dynamic RAM" in IEDM Tech. Dig., 1985(This issue).

(2) H.Sunami, T.Kure, Y.Yagi, K.Yamaguchi, and S.Shimizu;"Scaling Consideration and Dielectric Breakdown improvement of Corrugated Capacitor Cell (CCC) for future DRAM", in IEDM Tech. Dig., pp.232-235, 1984.

(3) S.Nakajima, T.Kure, K.Minegishi, K.Miura, T.Morie, M.Kimizuka, and T.Mano;"A Submicrometer Megabit DRAM Process Technology Using Trench Capacitors";IEEE Trans. Electron Devices, vol. ED-32, pp. 210-216,1985.

(4) N.Lifshitz, J.Electrochem. Soc., vol.130, p.1549, 1983.

(5) R.M.Levin and A.C.Adams;"Low Pressure Deposition of Phosphosilicate Glass Films", J.Electrochem.Soc., vol.129, p.1588 (1982).

(6) Y.Wada, D.A.Antoniadis;"Anomalous Arsenic Diffusion in Silicon Dioxide", J.Electrochem.Soc., p.1317(1981).